FPGA DESIGN AND IMPLEMENTATION OF A REAL-TIME VISION BASED LANE DEPARTURE WARNING SYSTEM

[1]Yu-Ren Lin (林昱仁), [2]Yi-Feng Su (蘇一峰)

[1] R&D Division of Automotive Research and Testing Center, Chunghua
[2] R&D Division of Automotive Research and Testing Center, Chunghua
E-mail: ericlin@artc.org.tw

ABSTRACT

Using a vision-based solution in intelligent vehicle application often requires large amounts of memory to handle the video stream and image process, which increases the complexity of the hardware and software. In this paper, we present a Field-programmable Gate Array (FPGA) implementation of a vision-based lane departure warning system. By taking video frames, the line gradient is estimated and the lane marks are found. By analyzing the position of the lane mark, the departure of the vehicle will be detected in time. This idea has been implemented in Xilinx Spartan6 FPGA. The lane departure warning system uses 39% logic resources and no memory of the device. The average availability is 92.5%. The frame rate is 30 frames per sec (fps).

Keywords *FPGA; Lane Departure Warning System*

1. INTRODUCTION

Within the last few years, as growth of the population of vehicles, the traffic accidents also become more and more serious. In order to increase the automobile safety, Intelligent Transportation (ITS) and Advanced Safety Vehicle (ASV) are developed. One of these important achievements is vehicle safety system with image processing technology. Most occurrences of accidents results from the distracted driving and inattentive driving. When driver becomes tired or distracted, vehicle might move out if its lane. This critical situation often procures a serious accident. To avoid this critical situation, Lane Departure Warning System (LDWS) is developed. When vehicle prepares to move out of its lane on free way or arterial roads, the system will warn the driver.

The technologies of finding the lane marks are needed by the LDWS. Compared with other technologies, vision based LDWS is a human decision-make like solution to avoid the accident cause by lane departure with low cost and high reliability. In such systems, one CCD/CMOS camera is installed in the interior of the vehicle and the environment is sensed to supply useful information.

There are several LDWS have been developed on variety technologies [1-9]. B.Yu, W.Zhang and Y.Cai [1] used a Gaussian template to remove the dirty spots in the image and dynamical threshold choosing to find lane marks.TLC and CCP method are used to make lane departure decision. Cl´audio and Christan[2] proposed a lane departure warning system that estimates lane orientation through linear parabolic model. P.Y.Hsiao, C.W.Yeh, S.S.Huang and L.C.Fu[3] proposed an embedded ARM-based real-time LDWS. 1-d Gaussian smoother and a global edge detector are adopted to reduce noise effects in the image and lane departure decision is based on spatial and temporal mechanisms.

W.Zhu, F.Liu, Z.Li, X.Wang and S.Zhang[4] proposed an algorithm to chooses a common curved lane parameter model which can describe both straight and curved lanes. N.M.Enache[5] used composite Lyapunov Functions, polydral-like invariant sets and linear matrix inequality(LMI) method to implement the lane-departure avoidance system. M.J Jeng[6] proposed a LDWS which is implemented in hardware and software. The hardware is implemented by FPGA. In software design, the global edge detection is able to transfer the gray level image to binary pattern and show the edge of object and then finding out the lane marks by peak finding and grouping, edge connecting, lane segment combination, lane boundaries selection. Because the lane marks are extracted based on color information, H.Y.Cheng[7] proposed a method to utilize size, shape, and motion information to find the lane mark out. A.AM.Assidiq[8] proposed a method to detect the lane mark by Canny edge detector and Hough Transform. J. F. Liu[9] used gradient to find out the both lane marks.

Using vision based solution often requires large memory to handle video data stream, image processing, which increase the complexity of hardware and software. Some of these functions might not be implement by DSP. Besides DSP solution often

increases the system greatly. Therefore, FPGAs are instead of DSP. Broadly speaking, a FPGA implement can offer more functionality and be a lower–cost solution than DSP design[10].

The approach of this paper is extension of research by J. F. Liu[9] ,and organized into 4 sections. The basic processing step is introduced in section 2. The FPGA architecture is introduced in section 3. Section 4 presents the experimental results and implementation results.

2. ALGORITHM OF LANE RECOGNITION

All steps in the algorithm are shown in figure 1.

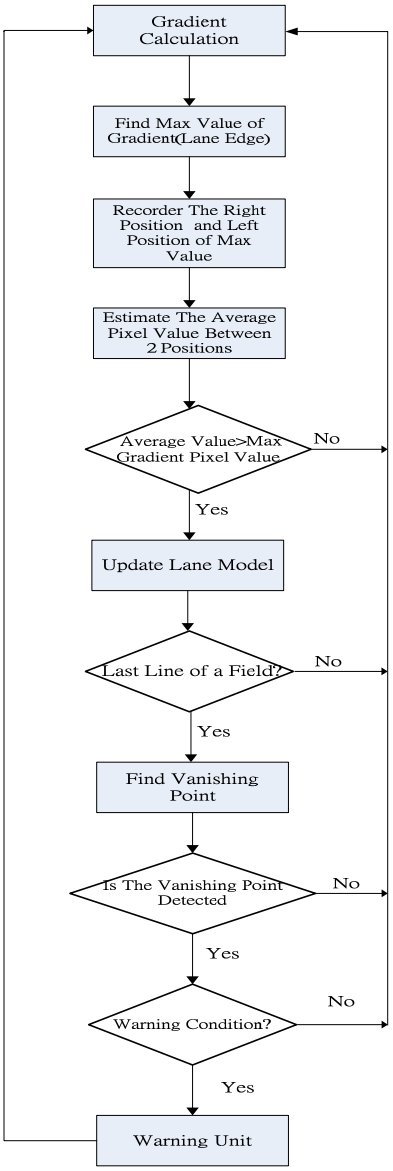

Figure 1: Flowchart of lane detection

The proposed lane marks detection algorithm is based on line gradient estimation method. All of the lane marks in the roadway image have higher gray values than surface. Therefore, the line gradient can be estimated by equation (1):

$$G_i = -P_{i-1} + 2 \times P_i - P_{i+1} \quad (1)$$

Wherein, Gi is the line gradient value of position i in the image. Pi is the pixel value in the image's region of interest. The edge of every lane marks can be detected by finding the max value of Gi. Continuity is an important cue to identify whether the region between boundaries is a lane mark or not. The average pixel value is used to identify if there is continuity between the region of right boundary and left boundary.

After finding the edge of one lane mark, the middle position of a lane will also be found. Recursive Least Square method and the middle positions are used to build the lane model.

$$L_{N+1} = P_N X_{N+1}[1 + X^T_{N+1} P_N X_{N+1}]^{-1} \quad (2)$$

$$P_{N+1} = [I - L_{N+1} X^T_{N+1}] P_N \quad (3)$$

$$\beta_{N+1} = \beta_N + L_{N+1}[y_{N+1} - X^T_{N+1}\beta_N] \quad (4)$$

Where $X_{N+1} = \begin{bmatrix} x_{N+1} \\ 1 \end{bmatrix}$

$$P_N = (X^T_N X_N)^{-1}$$

$$\beta_N = \begin{bmatrix} a_N \\ b_N \end{bmatrix}$$

According equation (2), (3) and (4), the matrix of lane model will be defined as equation (5).

$$y = a_N x + b_N \quad (5)$$

The abscissa of vanishing point y and the ordinate of vanishing point x will be defined as equation (6) and (7).

$$x = \frac{a_r - a_l}{b_l - b_r} \quad (6)$$

$$y = \frac{a_r (a_r - a_l)}{b_l - b_r} + b_r \quad (7)$$

As shown as figure 2, when both lane marks are detected, the vanishing point will be in the detecting region.

Figure 2: Software result of lane detection

The lane departure offset estimation method is shown in figure 3 and the slope of lane can be found by equation (5). Then the distance between the vehicle and the lane ΔX can found by equation (8) and (9).

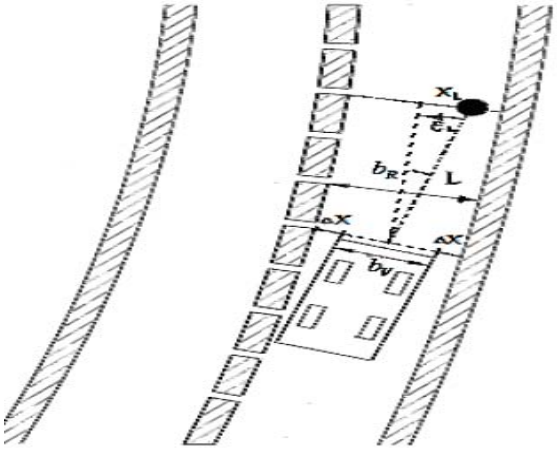

Figure 3: Method of Lane Departure Estimation

$$\Delta X_L = \frac{b_R}{2} - (\frac{b_V}{2} + X_L) \quad (8)$$

$$\Delta X_R = \frac{b_R}{2} - (\frac{b_V}{2} - X_L) \quad (9)$$

If the distance ΔX is larger than the threshold, the vehicle moves out of the lane.

3. FPGA IMPLEMENT OF LANE DETECTION ALGORITHM

The block diagram of proposed lane detection algorithm is shown in Figure 4, which consists of five main parts: a line gradient estimation unit, pixel sum and pixel average estimation unit, a max gradient position estimation unit, right lane and left lane model estimation unit, and vanishing point estimation unit.

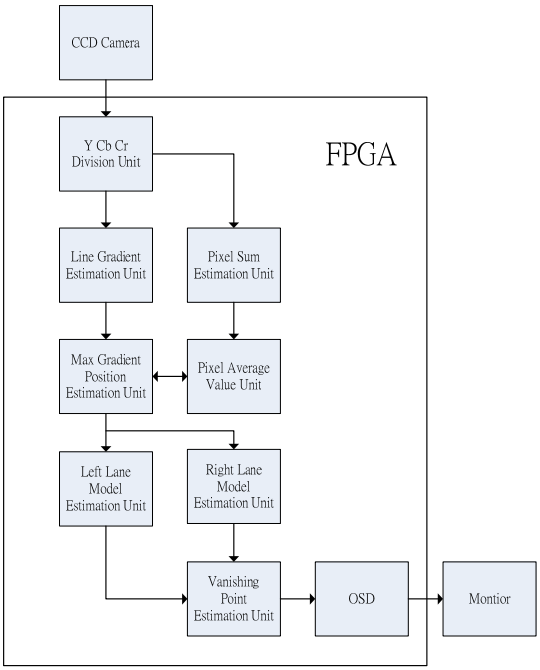

Figure 4: Block diagram of proposed lane detection algorithm

3.1. Line Gradient Estimation Unit

The architecture of the line gradient estimation unit is shown as figure 5.

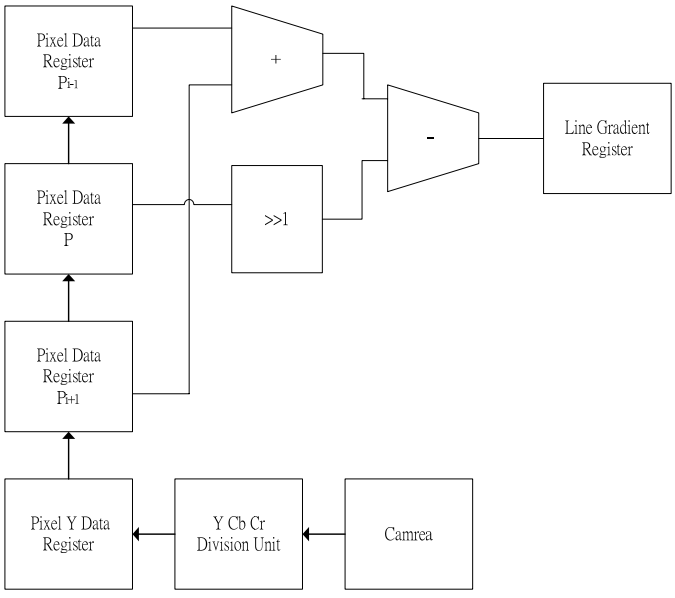

Figure 5: Architecture of the line gradient estimation unit

In order to reduce the required memory, all of the data are estimated in real time. First, the Y Cb Cr division unit outputs Y data to the pixel data register Pi+1. Next, the pixel data which is in the pixel register

Pi+1 will shift to register Pi and new pixel data from Y data register will be stored in register Pi+1. Pixel data register Pi-1 will receive pixel data and line gradient will be estimated until the next clock cycle. After calculating the line gradient, these data will be stored in line gradient register.

3.2. Max Gradient Position Estimation Unit

In this unit, the line gradient will shift from one gradient register to the next register, the left and right max gradients will be found. One register can represent one position. For example, if max gradient is in the gradient register 4, the max gradient position is 5. According to the lane width, the distance between the right and left max gradient position can be defined. One look up table is used to define the lane width.

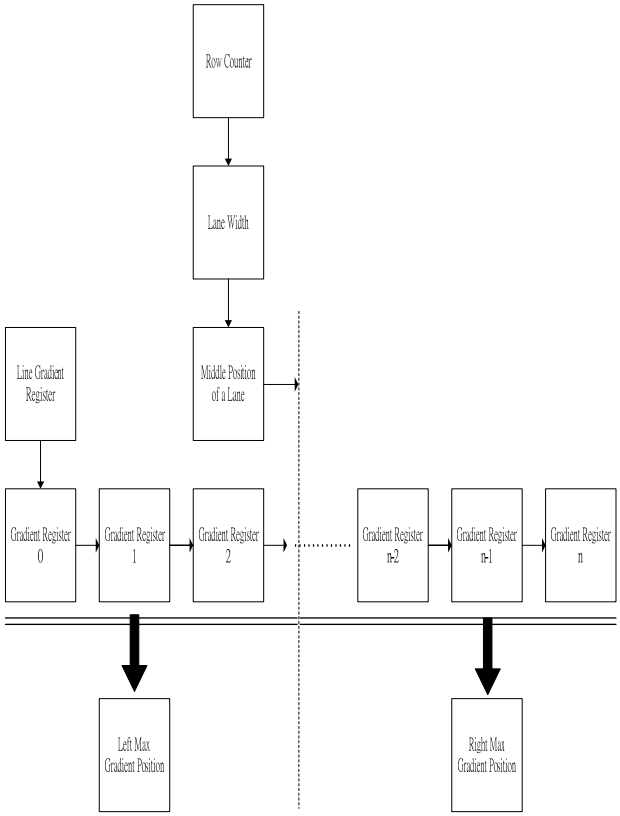

Figure 6: Architecture of the max gradient position estimation unit

3.3. Pixel Sum And Pixel Average Unit

In order to identify the distance between the right and left max gradient position is the boundary of a lane mark, the pixel average is needed. If the average larger than the pixel value which is in the right and left position, the boundary of a lane mark can be found.

3.4. Lane Model Estimation Unit

According to equation (2), (3) and (4), the steps of RLS algorithm can be defined as figure 6. The first position and the second position are used to estimate initial matrix P0 and β0. Matrix L, β, and P will be updated until both lane marks are not detected.

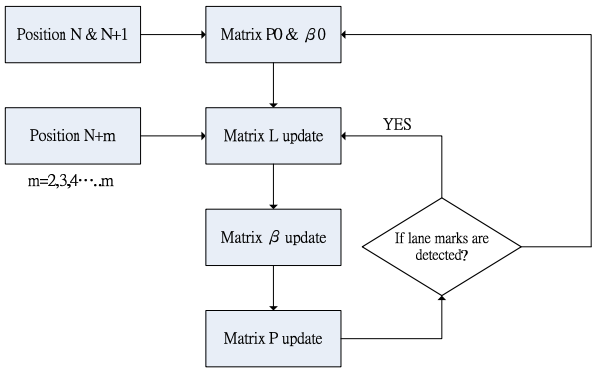

Figure 7: Steps of RLS algorithm

3.5. Vanishing point estimation unit

In this unit, equation (6) and (7) is implemented to calculate the abscissa y and the ordinate x. If the x and y are in the detecting area, both lane marks are detected. The displacement of vehicle ΔX can be define by equation (8) and (9). . If values of ΔX larger than the alert limit set by user, the user is alerted by a LED, a buzz or a speaker.

4. IMPLEMENT RESULTS AND EXPERIMENTAL RESULTS

4.1. Implement Result

Our goal is to implement a real-time lane departure warning system in FPGA. The system has been successfully implemented and tested on the SPARTAN6 XC6SLX150 FPGA. The utilization of the device is shown in Table 1.

Table1: Resource Utilization of Device (XC6SLX150)

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	10,791	184,304	5%
Number of Slice LUTs	27,699	92,152	30%
Number used As logic	26,884	92,152	29%
Number of Occupied Slices	8992	23,038	39%

The lane departure warning system use 39% logic resources and no block memory of the device.

4.2. Experimental results

In this section, the LDWS was verified by using the video database. Our experimental environment is based on the FPGA kit as figure 7. The verifiable video is stored in portable video recorder, played in the form of NTSC and input to the FPGA.

Figure 8: The Xilinx Spartan 6 FPGA kit

The video includes various situations (eg. daytime, nighttime, highway and urban road).The picture of test results is shown as figure 8.If both lane marks are detected, two green lines and a square will be shown in the screen. Both green lines are the lane marks and the midpoint of the square is the vanishing point of both lane marks. If the departure of vehicle is detected, the green lines and square will turn to red. The system availability is listed in Table 2. The average availability is 92.5%.

Figure 9: Picture of test results

Table 2: System availability

Testing Condition Used	System Availability
Highway in the daytime	97%
Urban road in the daytime	89%
Highway at night	94%
Urban road at night	90%
Average availability	92.5%

According to the experimental results, we can summarize the following point:

(1) The system can be used under various vehicles and environments in highway and urban road.
(2) The system can provide high availability, reliability and accuracy in lane deviation.
(3) The frame of system is more than 30 fps (frame per second), and it meets the requirement of real-time computing.
(4) 39% resource of a small FPGA and no memory is used to implemented the system.

5. CONCULSION

Compared to traditional DSPs and MCUs, FPGA offers faster processing speed and lower cost. The research proposed FPGA architecture of lane departure warning system and implement the system in FPGA. The system uses 39% logic resources and needs no memory of the FPGA. And the frame rate is more than 30 frames per second. The average availability of the LDWS is 92.5%. In the future, the architecture would be implemented by ASIC for lower cost.

REFERENCES

[1] B. Yu, W. Zhang, Y. Cai "A Lane Departure Warning System based on Machine Vision" in IEEE Pacific-Asia Workshop on Computational Intelligence and Industrial Application, 2008, pp.197-201.

[2] C.R. Jung, C.R. Kelber "A Lane Departure Warning System Using Lateral Offset with Uncalibrated Camera"

in Proc. Int. IEEE Conf. on Intelligent Transportation Systems, Sep. 13–16, 2005, pp. 348-353.

[3] P. Y. Hsioa, C. W. Yeh, S. S. Huang, L. C. Fu "A Portable Vision Based Real-Time Lane Departure Warning System : Day and Night", IEEE Trans. Intelligent Transportation Systems, vol. 58, no. 4, pp. 2089-2094, May 2009.

[4] W. Zhu, F. Liu, Z. Li, X. Wang, S. Zhang "A Vision Based Lane Detection and Tracking Algorithm in Automatic Drive", in IEEE Pacific-Asia Workshop on Computational Intelligence and Industrial Application, 2008, pp.799-803..

[5] N. M. Enache, S. Mammar and M. Netto, B. Lusetti "Driver Steering Assistance for Lane-Departure Avoidance Based on Hybrid Automata and Composite Lyapunov Function" in IEEE Trans. On Intelligent Transportation Systems, Mar. , 2010, vol1, pp.28-39.

[6] M. J. Jeng, C. Y. Guo, B. C. Shiau and L. B. Chang, "Lane Detection System Based on Software and Hardware Codesign," in Proc. 4th Int. IEEE Conf. on Autonomous Robots and Agents, Feb. 10-12, 2009, pp. 319 - 323.

[7] H. Y. Cheng, B. S. Jeng, P. T. Tseng, K. C. Fan, "Lane Detection With Moving Vehicles in the Traffic Scenes," in IEEE Trans. on Intelligent Transportation Systems, Vol.7 Dec. 2006, pp. 571-582.

[8] A. AM. Assidiq, O. O. Khalifa. Md. R. Islam, S. Khan, "Real Time Lane Detection for Autonomous Vehicles", in Proc. Int. IEEE Conf. on Computer and Communication Engineering, May. 13-15, 2008, pp. 82 – 88.

[9] J. F. Liu, Y.F. Su, M. K. Ko and P. N. Yu "Development of a Vision-Based Driver Assistance System with Lane Departure Warning and Forward Collision Warning functions" Digital Image Computing: Techniques and Applications, 2008, pp. 480–485.

[10] Sudhir Sharma, Wang Chen, "Using Model-Based Design to Accelerate FPGA Development for Automotive Applications", in 2009 SAE World Congress, January 1-15,2009.